RESEARCH SUMMARY

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Our group's current research interest is in the field of nanostructured semiconductor materials and devices. Our approach is to innovate at the level of materials and structures and discover radically new device concepts to enable revolutionary advances in several areas of science and technology, ranging from electronics and photonics, to energy and medicine. Scalability, integrability, and versatility are essential parts of our methodology in the acceleration of fundamental nanoscale scientific concepts into engineering solutions. We have developed a multifaceted research program that is vertically integrated from crystal growth to device design, fabrication and characterization; and laterally cross-disciplinary in nature. Our program encompasses III-V compound semiconductor epitaxial growth by metalorganic chemical vapor deposition (MOCVD), innovative fabrication approaches combining top-down fabrication and bottom-up self-assembly, 3D nanoscale active and passive electronic and photonic devices, and recently, an exciting new direction that takes advantage of one of our nanotechnology platforms, for neural regeneration.

Below are brief summaries of four of our research portfolios:

●**III-V planar nanowire based HEMT by MOCVD: a monolithic III-V nanowire array platform for high frequency low power electronics.** Analogous to the digital success story culminating with Si 3D CMOS, the RF sector is dominated by III-V high electron mobility transistors (HEMTs). III-V HEMTs are the preferred platform for RF applications because of the high electron velocity in the undoped channel over MESFETs and MOSFETs. It is therefore highly desirable to adopt a version of the 3D MOSFET using a HEMT structure for high-frequency RF performance. However, using a conventional top-down fabrication process to realize a 3D III-V HEMT would require a wrap-style heterojunction to form a 3D quantum well after etching the 3D channel (fin). This requires ex-situ epitaxial growth of the top barrier to the exposed 3D fins with sidewall etch damage in addition to surface oxidation, dangling bonds, and a non-abrupt interface at the heterojunction. Because of challenges, most reported performance is based on "nano ribbons" with a 2D electron gas (2DEG) only at the top facet. As a result, HEMTs with 3D III-V topologies largely remain unexplored.

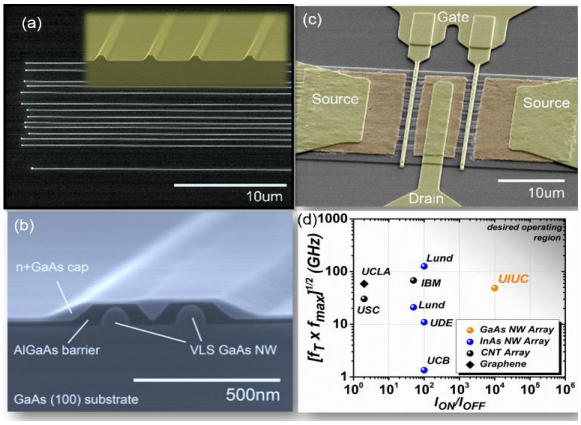

Fig. 1 Planar III-V nanowire platform for nanoelectronics. (a) Top and cross-sectional (inset) views of site-controlled planar GaAs nanowire array; (b) monolithically grown HEMT structure with two planar GaAs nanowires in the channel (Miao et al. ; (c) fully fabricated HEMT structure with parallel NWs spanning both gate fingers in the RF probe layout; and (d) performance benchmark with other bottom-up grown nanowire or nanotube array based device results (*Miao, Chabak, et al. Nano Lett. 2015, and references therein*).

Our lab's discovery of parallel arrays of planar III-V nanowire growth mode (*Nano Lett. 8, 4421 (2008)*) has completely transformed the long-standing misperception of uncontrollability of self-assembled nanowires. On the fundamental side, this work opens up a new paradigm of crystal growth: selective lateral epitaxy (*Nano Lett. 14, 6836 (2014)*) and consequently in situ lateral junctions (*Choi et al. submitted*). Technologically, in-plane nanowire configuration is perfectly compatible with

existing planar processing technology for industry. We have demonstrated chip-scale transistors (HEMTs) with record DC and RF performance (*Nano Lett. 15, 2780 (2015)*). A clear path that includes developing heterogeneous nanowire selective lateral epitaxy (*IEEE Electron Dev. Lett. 36, 633 (2015)*) with extremely high density for reduction of parasitic capacitance and increase mobility is established to reach THz for high speed applications. This work provided the first unambiguous evidence for the engineering potential of bottom-up grown nanowires. Future work will include heterogeneous integration of the nanowire array onto silicon and flexible substrates for beyond Si CMOS logic (*IEEE Trans. Electron Dev. 63, 223 (2016)*) and future III-V RF electronics (*IEEE Electron Dev. Lett. 36, 445 (2015)*), as well as optoelectronic applications.

This work has resulted in numerous invited presentations, including plenary and keynote lectures at nanowire related workshops and conferences. Aspects of this research have been supported by NSF ECCS, NSF DMR, DARPA, ONR, and Intel etc.

●**Strain-induced self-rolled-up membrane (S-RuM) nanotechnology – a new degree of freedom and a new potentially disruptive platform for advanced 3D devices for passive electronics and neural biology.** Complex 3D structures enable efficient use of materials leading to advanced functionalities that are otherwise out of reach. However, if conventional fabrication technologies are used to process 3D structures, issues such as mechanical stability, conformity, alignment, as well as cost, are difficult to address. The self-rolled-up membrane (S-RuM) technology, that we have been developing, aims to ensure that achieving 3D functional hierarchical architectures without the difficulties of processing in 3D is by no means an incompatible goal. The overarching physical principle of S-RuM nanotech is strain-driven spontaneous deformation of 2D membranes into 3D architectures (*J. Phys. D 41, 193001 (2008)*). This potentially disruptive platform has been demonstrated in our lab for extreme miniaturization and performance enhancement for various applications including extremely miniaturized high frequency (5G) passive electronics and intelligent synthetic neural circuits.

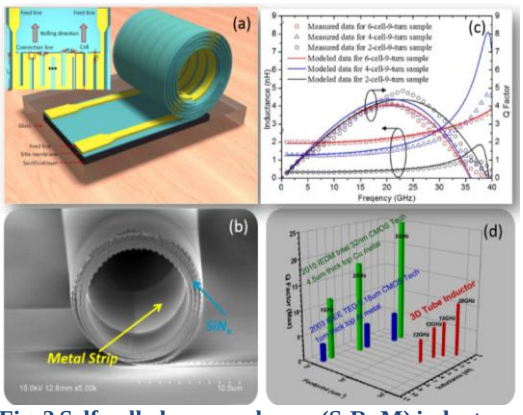

Fig. 2 Self-rolled-up membrane (S-RuM) inductors: extreme miniaturization and high frequency 3D passive electronics. (a) Schematic of the S-RuM inductor concept, (b) fabricated rolled inductor with 9-turns, (c) experimental and simulated electrical performance of various rolled inductor configurations, and (d) benchmark chart with planar counterparts. *Yu, Huang, et al. Sci. Rep. 2015, and references therein.*

The S-RuM inductors our lab has demonstrated has a form factor that is 10 – 100 times smaller than the 2D counterpart (*Sci. Rep. 5, 9661 (2015) and Nano Lett. 12, 6283 (2012)*). By virtual of the small size and 3D confinement, energy loss to substrate and free space is minimized, leading to high frequency operation. **Fig. 2** highlights the concept and performance of rolled-up inductors, consisting of rolled-up 100 nm-thick interconnected parallel Au lines (and Cu lines in the near future) supported by the strained SiN_x membrane. In contrast to a planar counterpart, this 3D platform promises to make IC chips that are extremely small and light, with dramatically enhanced inductance density, superior Q/frequency, minimized substrate integration, and, at the same time, reduction of the fabrication cost per chip, especially when the S-RuM methodology is extended to other passives.

By stacking two S-RuM inductors in-plane or vertically to form transformers (*Patent # 8,941,460*) we have also achieved near unity coupling coefficients and unprecedentedly-high turn-ratios (>36). Through global and local strain engineering, S-RuM filters (*Pending Patent #62/144,516*), transmission lines (*Patent #9,018,050*), antennas with ultra-high frequency (including THz) and bandwidth (*Pending Patent #62280160*) can all been enabled. S-RuM technology is a potentially

disruptive technology, particularly in the emerging CMOS millimeter wave wireless communications markets.

Recently, together with our collaborators in biomedical engineering, we have embarked on an uncharted territory – neural regeneration. We have demonstrated that the silicon nitride based S-RuM microtube array serves as an excellent cortical neuron cell culturing platform that provided unprecedented spatial guidance and acceleration for the growing axons: Froeter et al. "Toward Intelligent Synthetic Neural Circuits: Directing and Accelerating Neuron Cell Growth by Self-Rolled-Up Silicon Nitride Microtube Array," *ACS Nano, 8 (11), 11108 (2014)*. Further studies to explore the full potential of S-RuM platform as an active neural interface are underway.

This work has resulted in 3 issued and 4 pending patents. Aspects of this research portfolio have been supported by NSF ECCS, NSF ERC, DARPA, and DOE, as well as internal college of engineering awards and initiatives.

●**Metal Assisted Chemical Etching (MacEtch) - powerful nanofabrication technology that defies textbooks, and now in 3D controlled by magnetic field.** Metal assisted chemical etching (MacEtch) is a *directional wet* etch method, that defies the isotropic nature of wet etch through local catalysis effect and enables site-controlled semiconductor nanostructure fabrication with unpresented aspect ratio (>> 100:1) and versatility (*Curr. Opin. Solid State Mater. Sci. 16, 71 (2012)*). This invention impacted the field in a profound way, not only because of the readily achievable extraordinary aspect ratio, but also the absence of ion-induced damage. Prof. Li's first paper (*Appl. Phys. Lett. 77, 2572 (2000)*) on this discovery has been already cited 730 times according to Google Scholar. Five related patents have been issued and more than three are pending. Our lab continues to push the frontiers of this technology by investigating the fundamental mechanism and properties of MacEtch and extending its applicability to compound semiconductors, including Si, III-As, III-P, III-N, SiC, and Ga_2O_3 with unprecedented aspect ratio. We have achieved atomically smooth sidewalls bypassing the metal catalyst edge roughness through inverse-MacEtch (***i-MacEtch***, *Nano Lett. 15, 641 (2015)*) and arbitrary direction etching through programmable magnetic-field guidance (***h-MacEtch***, *Appl. Phys. Lett. 103, 214103 (2013) and ongoing studies*), as well as CMOS compatible metal catalysts, as highlighted in **Fig. 3**. We have also validated the technical relevance of MacEtch by demonstrating LEDs (*J. Appl. Phys. 114, 064909 (2013)*), transistors (*IEEE Electron Dev. Lett. 37, 970 (2016)*), solar cells (*IEEE J. Photovol. 2, 129 (2012)*), thermoelectrical devices (*Nano Lett. 15, 3159 (2015)*), photonic crystals (*Appl. Phys. Lett. 103, 214103 (2013)*), and plasmonics (*Adv. Mater. 28, 1441 (2016)*), which otherwise can either only be fabricated by reactive ion etching (RIE) or not possible at all.

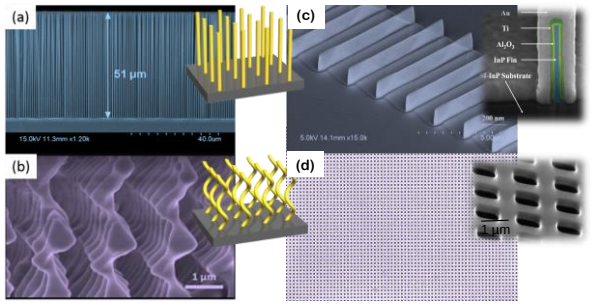

Fig. 2 Programmable anisotropic metal-assisted chemical etching (MacEtch). (a) Si nanowire array with 100: 1 aspect ratio (*Balasundaram et al. Nanotech. 2012*); (b) GaAs nanowire array with etching directions modulated (*Dejarld et al. Nano Lett. 2011*). (c) InP fin array by inverse-MacEtch. Inset shows a fully fabricated InP finFET with 14 nm gate width (*Song et al. IEEE EDL 2016*). (d) Si photonic crystal reflector (*Balasundaram et al. APL 2013*).

The simplicity, versatility, manufacturability, and realistic potential of MacEtch to replace and enhance dry etch methods for various applications have been widely recognized by the community. While NSF is sponsoring certain fundamental aspects of this innovation including the full programmability Several companies, including SanDisk and Lam Research, have been sponsoring our research aiming to commercialize this technology for future generation through-silicon-vias (TSVs), memory, thermoelectric, and photovoltaic devices.

● **Heterogeneous integration of III-V with Si and 2D van der Waals sheets: breaking the lattice mismatch barrier, van der Waals epitaxy, tandem solar cells and most recently, single sheet laser for attojoule optoelectronics.** III-V compound semiconductors have enabled an entire optoelectronic industry including lasers, LEDs, and solar cells; and are widely regarded as the most promising candidates for beyond silicon CMOS electronics. However, the paramount obstacle to achieve high quality heterojunctions with the desired band alignment, which are critical to carrier diffusion and injection efficiencies, is the non-ideal interfaces due to the lattice mismatch in epitaxial growth and surface passivation issues. Breaking the lattice match barrier through lateral strain relaxation, we have demonstrated the integration of III-V ($In_xGa_{1-x}As$ and $GaAs_yP_{1-y}$) nanowires on silicon through both selective area epitaxy (*App. Phys. Lett. 106, 133102 (2015)*) and direct epitaxy (*ACS Nano 7, 5463 (2013) and Nano Lett. 11, 483 (2011)*) by MOCVD. We have achieved III-V nanowire/Si interface quality that enabled reasonable performance solar cells (*ACS Nano 6, 11074 (2012),* with a direct path to triple junction tandem cells. Ultimately, more "perfect" interfaces may be achieved through van der Waals epitaxy on 2D van der Waals (vdW) sheets (e.g. MoS_2 and other TMDCs), where there are no dangling bonds at the surface. Furthermore, combining III-V compound semiconductors with semiconducting 2D vdW monolayers will create new possibilities in band structure engineering with significantly relaxed lattice matching requirements. We have discovered the spontaneous phase segregation phenomenon driven for lattice matched van der Waals epitaxy (*Nano Lett. 13, 1153 (2013)*) through the growth of $In_xGa_{1-x}As$ nanowires on graphene and other 2D sheets (**Fig. 4a**). We have then successfully grown single-phase ternary InGaAs nanowires and core-shell p-n junction solar cells, by inserting an InAs segment in between graphene and InGaAs (*Adv. Mater. 26, 3569 (2014)*). The direct epitaxy on graphene platform established through this work has significant implications for a wide variety of III-V compound semiconductor NW based devices on graphene, such as light emitters and multi-junction tandem solar cells, all of which can also be released for applications that requires flexible form factors.

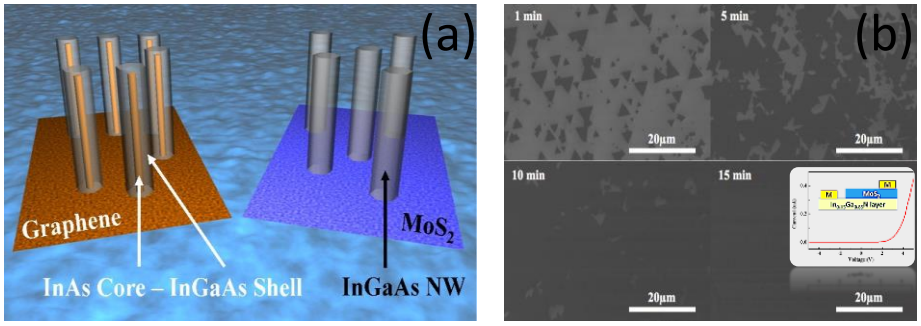

Fig. 3 III-V/2D and 2D/III-V van der Waals heterogeneous epitaxy. (a) Schematic illustration of spontaneous InGaAs nanowire phase segregation on graphene, but not on MoS_2, driven by the close lattice match between InAs and graphene (*Mohseni et al. Nano Lett. 2013*). (b) SEM images showing the evolution of MoS_2 vdW epitaxy on GaN to form a continuous sheet, as a result of the epitaxial alignment. Inset shows the IV characteristics of a p-InGaN/n-MoS_2 diode (*Jung et al. IEEE IPC 2016*).

Recently, we have started investigating the van der Waals epitaxy of TMDCs on III-N structures for large area high quality monolayer formation (**Fig. 4b**). Coupled with optical cavity design for enhanced light-matter interaction, together with our collaborators and supported by AFOSR, we are exploring integration schemes towards 2D sheet lasers for demonstration of enhanced light emission and lasing from monolayer 2D materials, with both optical pumping and electrical injection.

In summary, our research focuses on developing innovative semiconductor structures and device concepts through both bottom-up and top-down approaches to bring lasting impact to the field of semiconductor nanotechnology, electronics, and photonics; and possibly to medicine in the future.